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Description

METHOD FOR CO-LAYOUT OF DIFFERENT BUSES IN AN ELECTRIC BOARD

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a structure for reducing cross-talk, and more particularly, to a different-buses-co-layout structureutilizing a plurality of non-operating buses as shielding traces to reduce cross-talk.

[0003] 2. Description of the Prior Art

[0004] When a novel technique replaces a conventional technique, there are transitional commercialized products on the market, such as an electric board conforming to both SDR (Single Data Rate) and DDR (Double Data Rate) specifications. To save costs conforming to both the new and old specifications, designers strive to integrate the new and old related devices in one electric board. Taking

memory devices in a computer as an example, when DDRII is being promoted and DDRIis not yet phased out, designers will try to integrate the DDR I and the DDR II in the same motherboard. However, when hardware devices and corresponding buses respectively conforming to different specifications are co-laid out in the same motherboard, the cross-talk effect appears and designers have to come up with cost-effective and efficient methods to reduce the cross-talk effect.

[0005] Many prior-art patents disclose a ground-shielding characteristic in a structure laid out with buses of the same type. In brief, a plurality of ground traces are interlaced among signal lines with signals transmitted inside so that a ground shielding trace exists between every two signal lines to avoid the signal interference. In US Patent No. 6,444,922,"Zero cross-talk signal line design", Kwong et al. etch thin slots at two sides of each signal line on the electric board to form a metal shield around each signal line. However, the above-mentioned prior-art technique will suffer an extremely high cost and not be practical for manufacturing. In addition, increasing the distance between every two signal lines will lead to an enlargement of the electric board and raise the cost.

[0006] Please refer to Fig.1 and Fig.2. Fig.1 is a schematic diagram of a layout structure showing the DDR I installed on a motherboard. Fig.2 is a schematic diagram of a layout structure showing the DDR II installed on a motherboard. The combination of Fig.1 and Fig.2 can be viewed as a schematic diagram of a prior-art different-buses-co-layout structure.

[0007] In Fig.1, the DDR I layout structure 10 includes an electric board 12 installed with a ground layer, a plurality of slots 14, and a plurality of buses 16. For sake of clearness of the diagram, only one bus 16 and two slots 14 are shown in Fig.1. The plurality of slots 14 can be used to detachably accommodate a plurality of corresponding DDR I adapting devices, and the bus 16 is electrically connected to the slot 14 for transmitting signals and data. A resistor Rtt, which is installed at an end of the bus 16 (behind the slot 14) and connected to a voltage Vtt, is used for impedance matching to erase reflecting waves and for reducing rising/falling time of the transmitted signals to increase data-access efficiency.

[0008] The DDR II layout structure 20 shown in Fig.2 also includes an electric board 22 installed with a ground layer, a plurality of slots 24, and a plurality of buses 26. Similar to

the embodiment shown in Fig.1, only one bus 26 and two slots 24 are shown in Fig.2. Please notice that the electric board 12 of the DDR I layout structure 10 shown in Fig.1 is the same as the electric board 22 of the DDR II layout structure 20 shown in Fig.2. In addition, the plurality of buses 16 in the DDR I layout structure 10 and the plurality of buses 26 in the DDR II layout structure 20 are alternately co-laid out in the same electric board. Therefore, the combination of Fig.1 and Fig.2 can be viewed as a schematic diagram of a different-buses-co-layout structure according to the prior art. Moreover, the resistor Rtt in the DDR I layout structure 10 shown in Fig.1 can be integrated into the whole structure of the DDR II layout structure 20 for erasing reflecting waves and for reducing rising/falling time of the transmitted signals to increase data-access efficiency.

[0009] Please continue to refer to both Fig.1 and Fig.2. The DDR I layout structure 10 and the DDR II layout structure 20 respectively include a DDR I controller 18 and a DDR II controller 28. The DDR I controller 18 and the DDR II controller 28 are respectively used to control operations of the DDR I layout structure 10 and the DDR II layout structure 20. When the DDR I layout structure 10 operates, the

prior-art DDR II controller 28 of the DDR II layout structure 20 will be electrically connected to the ground layer of the electric board 22. However, the slots 24 (two slots 24 shown in Fig.2) in the DDR II layout structure 20 are not connected to the ground layer. As such, the "ungrounded" slots 24 shown in Fig.2 will operate as antennas to receive signals from the buses 16 in the DDR I layout structure 10 and to emit related signals to interfere with the transmitted signals in the neighboring buses 16 in the DDR I layout structure 10. Similarly, when the DDR II layout structure 20 operates, the DDR I layout structure 10 is not totally grounded and will interfere with the original transmitted signals to cause serious cross-talk effect.

SUMMARY OF INVENTION

[0010] It is therefore a primary objective of the claimed invention to provide astructure for reducing cross-talk among adjacent signalsby utilizing a plurality of non-operating buses as shielding traces and to solve the above-mentioned problems.

[0011] According to the claimed invention, a structure for reducing cross-talk includes an electric board having a ground layer. A plurality of adapting modules are installed on the electric board such that only one adapting module oper-

ates at a time. Each adapting module has a plurality of slots for detachably accommodating a plurality of corresponding adapting devices and a plurality of buses electrically connected to the plurality of slots for transmitting signals and data. The plurality of buses of the plurality of adapting modules are alternately laid out on the electric board. When the adapting module does not operate, the corresponding plurality of buses are electrically connected to the ground layer of the electric board.

[0012] The claimed invention provides amethodfor reducing cross-talk in a different-buses-co-layout structure. The different-buses-co-layout structure comprises a plurality of buses for transmitting different types of signals and data. The method includes alternately laying out a plurality of buses of different types on an electric board, utilizing buses of only one type to transmit signals and data at any given time, and electrically connecting two ends of each bus not transmitting signals and data to a ground layer of the electric board.

[0013] According to the claimed invention, a different-buses-co-layout structure for reducing cross-talk includes an electric board having a ground layer and a first adapting module and a second adapting module installed

on the electric board. The two adapting modules cannot operate at the same time. Each adapting module includes a controller for controlling operations of the adapting modules. The controller has a MOS circuit for switching the controller between a predetermined voltage mode and a ground voltage mode so that when the adapting module does not operate, the MOS circuit switches the controller to the ground voltage mode. Each adapting module also includes a plurality of slots for detachably accommodating a plurality of corresponding adapting devices and a plurality of buses electrically connected to the plurality of slots for transmitting signals and data. The plurality of buses of the two adapting modules are alternately laid out on the electric board. When the adapting module does not operate, the corresponding plurality of buses is electrically connected to the ground layer of the electric board.

[0014] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the various figures and drawings.

Brief Description of Drawings

[0015] Fig.1 is a schematic diagram of a layout structure showing

the DDR I installed on a motherboard.

[0016] Fig.2. is a schematic diagram of a layout structure showing the DDR II installed on a motherboard.

[0017] Fig.3 is a schematic diagram showing two similar memory devices and corresponding buses of different types are co-laid out on the same electric board.

[0018] Fig.4 is a schematic diagram of a practical embodiment of the structure shown in Fig.3.

[0019] Fig.5 is a flow chart of a method of the present invention related to the embodiment shown in Fig.3.

[0020] Fig.6 is a schematic diagram of an embodiment of a step shown in Fig.5.

[0021] Fig.7 is a schematic diagram of an embodiment of another step shown in Fig.5.

DETAILED DESCRIPTION

[0022] The structure and method used for reducing cross-talk of the present invention is mainly applied in a different-buses-co-layout structure, in which a plurality of similar hardware devices and corresponding buses of different types are co-laid out on the same electric board. Please refer to Fig.3 which is a schematic diagram showing two similar memory devices and corresponding buses of different types are co-laid out on the same electric

board.The present embodiment inherits partial characteristics of the prior-art embodiments shown in Fig.1 and Fig.2.

[0023] Please refer to Fig.3. The present embodiment includes two adapting modules 30, 40 installed on an electric board 32. Please notice that these two adapting modules 30, 40 do not operatesimultaneously. The two adapting modules 30, 40 are respectively a DDR I layout structure 30 and a DDR II layout structure 40. The DDR I and DDR II layout structures 30, 40 jointly include the electric board 32 installed with a ground layer, and the DDR I and DDR II layout structures 30, 40 respectively include a plurality of slots 34, 44 and a plurality of buses 36, 46. For sake of clearness of the diagram (Fig.3), only one bus 36 and two slots 34 are shown in the DDR I layout structure 30, and only one bus 46 and two slots 44 are shown in the DDR II layout structure 40.

[0024] Please refer to the DDR I layout structure 30 first, the two slots 34 can be used to detachably accommodate two corresponding DDRIadapting devices 35, and the bus 36 is connected to the two slots 34 for transmitting signals and data. The DDR I layout structure 30 further includes a DDR I controller 38 for controlling operations of the adapting

modules 30 and the DDR I layout structure 30. The DDR I controller 38 includes a MOS circuit, which is composed of a PMOS transistor and a NMOS transistor for switching the DDR I controller 38 between a predetermined voltage mode Vt and a ground voltage mode. In addition, a switch39 is installed at the end of the bus 36 (behind the slot 34) for switching the end of the bus 36 of the DDRI-adapting devices 35 between a predetermined voltage mode Vtt and a ground voltage mode. When being practically implemented, the resistor Rtt shown in Fig.1 for impedance matching can be included in the switch 39.

[0025] Please refer to the DDR II layout structure 40. The DDR II layout structure 40 includes a plurality of slots 44, and a plurality of buses 46. Similar to the embodiment of the DDR I layout structure 30, only one bus 46 and two slots 44 for accommodate corresponding DDRIIadapting devices 45 are shown. The DDR II layout structure 40 also includes a DDR II controller 48 for controlling operations of the adapting modules 40 and the DDR I layout structure 40. The DDR II controller 48 still makes use of a MOS circuit to switch the DDR II controller 48 between a predetermined voltage mode Vt and a ground voltage mode.

[0026] Please notice that the DDR I layout structure 30 and the

DDR II layout structure 40 jointly make use of the electric board 32, and the buses 36 of the DDR I layout structure 30 and the buses 46 of the DDR II layout structure 40 are alternately laid out on the electric board 32.

[0027] Please refer to Fig.4, which is a schematic diagram of a practical embodiment of the structure shown in Fig.3. When theDDR I layout structure 30 operates, the buses 36 of the DDR I layout structure 30 are used to transmit signals and data. However, due to the fact that the buses 36 andthe buses 46 are alternately laid out on the same electric board 32, the transmitted signals in the bus 36 of the DDR I layout structure 30 will interfere with the neighboring buses 46 of the DDR II layout structure 40.In addition, related electro-magnetic waves will return to interfere with the bus 36 with signals transmitted inside the buses 46. Similarly, when the DDR II layout structure 40 operates, cross-talk will happen.

[0028] The above-mentioned embodiment of the present invention can make use of ground shielding to eliminate cross-talk, and the basic principle is as follows. Please refer to Fig.5, which is a flow chart of a method of the present invention related to the embodiment shown in Fig.3.

[0029] Step 100: Alternately lay out the buses 36 of the DDR I

layout structure 30 and the bus 46 of the DDR II layout structure 40 on the electric board 32.

[0030] Step 101: Utilize the buses 36 or the buses 46 (corresponding to the DDR I or DDR II) to transmit signals and data, that is, the two adapting modules 30, 40 do not operate at the same time.

[0031] Step 102: When the DDR IIlayout structure operates, electrically connect two (terminal) ends of the buses 46 of DDR II layout structure to the ground layer of the electric board 32 to reduce cross-talk among the buses 36.

[0032] Step 103: When the DDR IIIlayout structure operates, electrically connect two (terminal) ends of the buses 36 of DDR I layout structure to the ground layer of the electric board 32 to reduce cross-talk among the buses 46.

[0033] Please refer to Fig.6, which is a schematic diagram of an embodiment of the step 102 shown in Fig.5. When theDDR I layout structure 30 operates (the slot 34 is installed with corresponding DDRIadapting devices 35), the switch 39 of the DDR I layout structure 30 will be connected to the predetermined voltage Vtt. In the non-operating DDR II layout structure 40, the slot 44 closest to the (terminal) end of the bus 46 is installed with a terminator card 47, which can connect the slot 44 to the

ground layer of the electric board 32. In the meantime, the MOS circuit of the DDR II controller 48 connects the DDR II controller 48 to the ground voltage (the PMOS transistor switches off and the NMOS transistor switches on), so that all the related traces of the DDR II layout structure 40 in the electric board 32 are grounded. In addition, due to the fact that the terminator card 47 is installed in the slot 44 closest to the (terminal) end of the bus 46, the bus 46 can be totally grounded to form a shielding trace to block any cross-talk.

[0034] Please refer to Fig.7, which is a schematic diagram of an embodiment of the step 103 shown in Fig.5. When the DDR II layout structure 40 operates (the slot 44 is installed with corresponding DDRIIadapting devices 45), the switch 39 of the non-operating DDR I layout structure 30 will be connected to the ground voltage and the MOS circuit of the DDR I controller 38 will connect the DDR I controller 38 to the ground voltage (the PMOS transistor switches off and the NMOS transistor switches on) so that all the related traces of the DDR I layout structure 30 in the electric board 32 are grounded.

[0035] The above-mentioned embodiments employ two adapting modules (the DDR I layout structure 30 and the DDR II

layout structure 40). However, when being practically implemented, the quantity of the adapting modules, the slots, and the buses should not be limited. The major characteristic of the present invention is to co-lay out buses of different types on the same electric board and to connect two ends of each non-operating bus to a ground layer of the electric board to form shielding traces to reduce cross-talk. Therefore, when different buses are co-laid out on the same electric board, there is no need to increase the distance between sets of buses and raising the cost.

[0036] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.